start\_gui

open\_project F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.xpr

open\_project F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.xpr

Scanning sources...

Finished scanning sources

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository 'F:/Xilinx/Vivado/2019.2/data/ip'.

open\_project: Time (s): cpu = 00:00:12 ; elapsed = 00:00:06 . Memory (MB): peak = 818.656 ; gain = 167.629

update\_compile\_order -fileset sources\_1

launch\_simulation

Command: launch\_simulation

INFO: [Vivado 12-5682] Launching behavioral simulation in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

INFO: [SIM-utils-51] Simulation object is 'sim\_1'

INFO: [SIM-utils-54] Inspecting design source files for 'regFile\_tb' in fileset 'sim\_1'...

INFO: [USF-XSim-97] Finding global include files...

INFO: [USF-XSim-98] Fetching design files from 'sim\_1'...

INFO: [USF-XSim-2] XSim::Compile design

INFO: [USF-XSim-61] Executing 'COMPILE and ANALYZE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xvlog --incr --relax -prj regFile\_tb\_vlog.prj"

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/regFile.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module regFile

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/regFile\_tb.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module regFile\_tb

run\_program: Time (s): cpu = 00:00:00 ; elapsed = 00:00:06 . Memory (MB): peak = 832.074 ; gain = 0.000

INFO: [USF-XSim-69] 'compile' step finished in '6' seconds

INFO: [USF-XSim-3] XSim::Elaborate design

INFO: [USF-XSim-61] Executing 'ELABORATE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xelab -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot regFile\_tb\_behav xil\_defaultlib.regFile\_tb xil\_defaultlib.glbl -log elaborate.log"

Vivado Simulator 2019.2

Copyright 1986-1999, 2001-2019 Xilinx, Inc. All Rights Reserved.

Running: F:/Xilinx/Vivado/2019.2/bin/unwrapped/win64.o/xelab.exe -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot regFile\_tb\_behav xil\_defaultlib.regFile\_tb xil\_defaultlib.glbl -log elaborate.log

Using 2 slave threads.

Starting static elaboration

Pass Through NonSizing Optimizer

WARNING: [VRFC 10-3091] actual bit length 32 differs from formal bit length 64 for port 'write\_data' [F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/regFile\_tb.v:26]

WARNING: [VRFC 10-3091] actual bit length 32 differs from formal bit length 64 for port 'read\_data1' [F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/regFile\_tb.v:30]

WARNING: [VRFC 10-3091] actual bit length 32 differs from formal bit length 64 for port 'read\_data2' [F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/regFile\_tb.v:31]

Completed static elaboration

Starting simulation data flow analysis

WARNING: [XSIM 43-4100] "F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/glbl.v" Line 6. Module glbl has a timescale but at least one module in design doesn't have timescale.

Completed simulation data flow analysis

Time Resolution for simulation is 1ps

Compiling module xil\_defaultlib.regFile

Compiling module xil\_defaultlib.regFile\_tb

Compiling module xil\_defaultlib.glbl

Built simulation snapshot regFile\_tb\_behav

\*\*\*\*\*\* Webtalk v2019.2 (64-bit)

\*\*\*\* SW Build 2708876 on Wed Nov 6 21:40:23 MST 2019

\*\*\*\* IP Build 2700528 on Thu Nov 7 00:09:20 MST 2019

\*\* Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.

source F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/xsim.dir/regFile\_tb\_behav/webtalk/xsim\_webtalk.tcl -notrace

INFO: [Common 17-186] 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/xsim.dir/regFile\_tb\_behav/webtalk/usage\_statistics\_ext\_xsim.xml' has been successfully sent to Xilinx on Sun Jul 4 19:36:58 2021. For additional details about this file, please refer to the WebTalk help file at F:/Xilinx/Vivado/2019.2/doc/webtalk\_introduction.html.

INFO: [Common 17-206] Exiting Webtalk at Sun Jul 4 19:36:58 2021...

run\_program: Time (s): cpu = 00:00:01 ; elapsed = 00:00:13 . Memory (MB): peak = 832.074 ; gain = 0.000

INFO: [USF-XSim-69] 'elaborate' step finished in '12' seconds

INFO: [USF-XSim-4] XSim::Simulate design

INFO: [USF-XSim-61] Executing 'SIMULATE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

INFO: [USF-XSim-98] \*\*\* Running xsim

with args "regFile\_tb\_behav -key {Behavioral:sim\_1:Functional:regFile\_tb} -tclbatch {regFile\_tb.tcl} -view {F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/top\_tb\_behav.wcfg} -log {simulate.log}"

INFO: [USF-XSim-8] Loading simulator feature

Vivado Simulator 2019.2

Time resolution is 1 ps

open\_wave\_config F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/top\_tb\_behav.wcfg

WARNING: Simulation object /top\_tb/clock was not found in the design.

WARNING: Simulation object /top\_tb/reset was not found in the design.

WARNING: Simulation object /top\_tb/result was not found in the design.

WARNING: Simulation object /top\_tb/x was not found in the design.

source regFile\_tb.tcl

# set curr\_wave [current\_wave\_config]

# if { [string length $curr\_wave] == 0 } {

# if { [llength [get\_objects]] > 0} {

# add\_wave /

# set\_property needs\_save false [current\_wave\_config]

# } else {

# send\_msg\_id Add\_Wave-1 WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window go to 'File->New Waveform Configuration' or type 'create\_wave\_config' in the TCL console."

# }

# }

# run 1000ns

INFO: [USF-XSim-96] XSim completed. Design snapshot 'regFile\_tb\_behav' loaded.

INFO: [USF-XSim-97] XSim simulation ran for 1000ns

launch\_simulation: Time (s): cpu = 00:00:10 ; elapsed = 00:00:24 . Memory (MB): peak = 850.922 ; gain = 18.848

set\_property top ALU\_tb [get\_filesets sim\_1]

set\_property top\_lib xil\_defaultlib [get\_filesets sim\_1]

set\_property top decode\_tb [get\_filesets sim\_1]

set\_property top\_lib xil\_defaultlib [get\_filesets sim\_1]

launch\_simulation

Command: launch\_simulation

boost::filesystem::remove: 另一个程序正在使用此文件，进程无法访问。: "F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/simulate.log"

run all

launch\_simulation

Command: launch\_simulation

boost::filesystem::remove: 另一个程序正在使用此文件，进程无法访问。: "F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/simulate.log"

launch\_simulation

Command: launch\_simulation

boost::filesystem::remove: 另一个程序正在使用此文件，进程无法访问。: "F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/simulate.log"

relaunch\_sim

suspend\_sim: Time (s): cpu = 00:00:01 ; elapsed = 00:00:08 . Memory (MB): peak = 860.633 ; gain = 0.000

Command: launch\_simulation -simset sim\_1 -mode behavioral

INFO: [Vivado 12-5682] Launching behavioral simulation in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

INFO: [SIM-utils-51] Simulation object is 'sim\_1'

INFO: [SIM-utils-54] Inspecting design source files for 'decode\_tb' in fileset 'sim\_1'...

INFO: [USF-XSim-97] Finding global include files...

INFO: [USF-XSim-98] Fetching design files from 'sim\_1'...

INFO: [USF-XSim-2] XSim::Compile design

INFO: [USF-XSim-61] Executing 'COMPILE and ANALYZE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xvlog --incr --relax -prj decode\_tb\_vlog.prj"

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module decode

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode\_tb.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module decode\_tb

INFO: [USF-XSim-69] 'compile' step finished in '3' seconds

Command: launch\_simulation -simset sim\_1 -mode behavioral

INFO: [Vivado 12-5682] Launching behavioral simulation in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

INFO: [USF-XSim-3] XSim::Elaborate design

INFO: [USF-XSim-61] Executing 'ELABORATE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xelab -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot decode\_tb\_behav xil\_defaultlib.decode\_tb xil\_defaultlib.glbl -log elaborate.log"

Vivado Simulator 2019.2

Copyright 1986-1999, 2001-2019 Xilinx, Inc. All Rights Reserved.

Running: F:/Xilinx/Vivado/2019.2/bin/unwrapped/win64.o/xelab.exe -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot decode\_tb\_behav xil\_defaultlib.decode\_tb xil\_defaultlib.glbl -log elaborate.log

Using 2 slave threads.

Starting static elaboration

Pass Through NonSizing Optimizer

Completed static elaboration

Starting simulation data flow analysis

WARNING: [XSIM 43-4100] "F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/glbl.v" Line 6. Module glbl has a timescale but at least one module in design doesn't have timescale.

Completed simulation data flow analysis

Time Resolution for simulation is 1ps

Compiling module xil\_defaultlib.decode

Compiling module xil\_defaultlib.decode\_tb

Compiling module xil\_defaultlib.glbl

Built simulation snapshot decode\_tb\_behav

run\_program: Time (s): cpu = 00:00:00 ; elapsed = 00:00:06 . Memory (MB): peak = 860.633 ; gain = 0.000

INFO: [USF-XSim-69] 'elaborate' step finished in '6' seconds

launch\_simulation: Time (s): cpu = 00:00:00 ; elapsed = 00:00:06 . Memory (MB): peak = 860.633 ; gain = 0.000

Vivado Simulator 2019.2

Time resolution is 1 ps

relaunch\_sim: Time (s): cpu = 00:00:02 ; elapsed = 00:00:18 . Memory (MB): peak = 860.633 ; gain = 0.000

close\_sim

INFO: [Simtcl 6-16] Simulation closed

launch\_simulation

Command: launch\_simulation

INFO: [Vivado 12-5682] Launching behavioral simulation in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

INFO: [SIM-utils-51] Simulation object is 'sim\_1'

INFO: [SIM-utils-54] Inspecting design source files for 'decode\_tb' in fileset 'sim\_1'...

INFO: [USF-XSim-97] Finding global include files...

INFO: [USF-XSim-98] Fetching design files from 'sim\_1'...

INFO: [USF-XSim-2] XSim::Compile design

INFO: [USF-XSim-61] Executing 'COMPILE and ANALYZE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xvlog --incr --relax -prj decode\_tb\_vlog.prj"

INFO: [USF-XSim-69] 'compile' step finished in '3' seconds

INFO: [USF-XSim-3] XSim::Elaborate design

INFO: [USF-XSim-61] Executing 'ELABORATE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xelab -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot decode\_tb\_behav xil\_defaultlib.decode\_tb xil\_defaultlib.glbl -log elaborate.log"

Vivado Simulator 2019.2

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Running: F:/Xilinx/Vivado/2019.2/bin/unwrapped/win64.o/xelab.exe -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot decode\_tb\_behav xil\_defaultlib.decode\_tb xil\_defaultlib.glbl -log elaborate.log

Using 2 slave threads.

Starting static elaboration

Pass Through NonSizing Optimizer

Completed static elaboration

INFO: [XSIM 43-4323] No Change in HDL. Linking previously generated obj files to create kernel

INFO: [USF-XSim-69] 'elaborate' step finished in '4' seconds

INFO: [USF-XSim-4] XSim::Simulate design

INFO: [USF-XSim-61] Executing 'SIMULATE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

INFO: [USF-XSim-98] \*\*\* Running xsim

with args "decode\_tb\_behav -key {Behavioral:sim\_1:Functional:decode\_tb} -tclbatch {decode\_tb.tcl} -view {F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/top\_tb\_behav.wcfg} -log {simulate.log}"

INFO: [USF-XSim-8] Loading simulator feature

Vivado Simulator 2019.2

Time resolution is 1 ps

open\_wave\_config F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/top\_tb\_behav.wcfg

WARNING: Simulation object /top\_tb/clock was not found in the design.

WARNING: Simulation object /top\_tb/reset was not found in the design.

WARNING: Simulation object /top\_tb/result was not found in the design.

WARNING: Simulation object /top\_tb/x was not found in the design.

source decode\_tb.tcl

# set curr\_wave [current\_wave\_config]

# if { [string length $curr\_wave] == 0 } {

# if { [llength [get\_objects]] > 0} {

# add\_wave /

# set\_property needs\_save false [current\_wave\_config]

# } else {

# send\_msg\_id Add\_Wave-1 WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window go to 'File->New Waveform Configuration' or type 'create\_wave\_config' in the TCL console."

# }

# }

# run 1000ns

Starting Decode Test

--------------------------------------------------------------------------------

addi zero, zero, 0

Time: 10

instruction: 00000000000000000000000000010011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 0

read\_sel2: 0

write\_sel: 0

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

addi a1, zero, -1

Time: 20

instruction: 11111111111100000000010110010011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0003

read\_sel1: 0

read\_sel2: 31

write\_sel: 11

wEn: 1

branch\_op: 0

imm32: 11111111111111111111111111111111

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

add a6, a1, a2

Time: 30

instruction: 00000000110001011000100000110011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 11

read\_sel2: 12

write\_sel: 16

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

sub a7, a2, a4

Time: 40

instruction: 01000000111001100000100010110011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 12

read\_sel2: 14

write\_sel: 17

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 001000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

slt a0, a1, a5

Time: 50

instruction: 00000000111101011010010100110011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 11

read\_sel2: 15

write\_sel: 10

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 000010

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

xor a4, a1, a5

Time: 60

instruction: 00000000111101011100011100110011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 11

read\_sel2: 15

write\_sel: 14

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 000100

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

and a3, a3, a1

Time: 70

instruction: 00000000101101101111011010110011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 13

read\_sel2: 11

write\_sel: 13

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 000111

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

addi a1, zero, 1536

Time: 80

instruction: 01100000000000000000010110010011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0604

read\_sel1: 0

read\_sel2: 0

write\_sel: 11

wEn: 1

branch\_op: 0

imm32: 00000000000000000000011000000000

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

sw a2, 0(a1)

Time: 90

instruction: 00000000110001011010000000100011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 11

read\_sel2: 12

write\_sel: 0

wEn: 0

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 1

wb\_sel: 0

--------------------------------------------------------------------------------

lw s2, 0(a1)

Time: 100

instruction: 00000000000001011010100100000011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 11

read\_sel2: 0

write\_sel: 18

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 1

--------------------------------------------------------------------------------

jal zero,128

Time: 110

instruction: 00000001010000000000000001101111

PC: 0114

JALR\_target: 0000

branch 0

next\_PC\_sel 1

target\_PC 012c

read\_sel1: 0

read\_sel2: 20

write\_sel: 0

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000010100

op\_A\_sel: 10

op\_B\_sel: 1

ALU\_Control: 011111

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

jalr ra,196(ra)

Time: 120

instruction: 00001100010000001000000011100111

PC: 0094

JALR\_target: 0154

branch 0

next\_PC\_sel 1

target\_PC 0154

read\_sel1: 1

read\_sel2: 4

write\_sel: 1

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000011000100

op\_A\_sel: 10

op\_B\_sel: 1

ALU\_Control: 111111

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

BEQ x1, x2

Time: 130

instruction: 00000000001000001000100001100011

PC: 0004

JALR\_target: 0154

branch 0

next\_PC\_sel 0

target\_PC 0014

read\_sel1: 1

read\_sel2: 2

write\_sel: 16

wEn: 0

branch\_op: 1

imm32: 00000000000000000000000000010000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 010000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

BEQ x1, x2 - taken

Time: 140

instruction: 00000000001000001000100001100011

PC: 0008

JALR\_target: 0154

branch 1

next\_PC\_sel 1

target\_PC 0018

read\_sel1: 1

read\_sel2: 2

write\_sel: 16

wEn: 0

branch\_op: 1

imm32: 00000000000000000000000000010000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 010000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

LUI rd, DEADB

Time: 150

instruction: 11011110101011011011000110110111

PC: 0000

JALR\_target: 0154

branch 0

next\_PC\_sel 0

target\_PC b004

read\_sel1: 0

read\_sel2: 10

write\_sel: 3

wEn: 1

branch\_op: 0

imm32: 11011110101011011011000000000000

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

AUIPC rd, DEADB (Note PC = 0004 to begin

Time: 160

instruction: 11011110101011011011000110010111

PC: 0004

JALR\_target: 0154

branch 0

next\_PC\_sel 0

target\_PC b008

read\_sel1: 27

read\_sel2: 10

write\_sel: 3

wEn: 1

branch\_op: 0

imm32: 11011110101011011011000000000000

op\_A\_sel: 01

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

$stop called at time : 170 ns : File "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode\_tb.v" Line 227

INFO: [USF-XSim-96] XSim completed. Design snapshot 'decode\_tb\_behav' loaded.

INFO: [USF-XSim-97] XSim simulation ran for 1000ns

launch\_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:11 . Memory (MB): peak = 865.594 ; gain = 0.000

close\_sim

INFO: [Simtcl 6-16] Simulation closed

launch\_simulation

Command: launch\_simulation

INFO: [Vivado 12-5682] Launching behavioral simulation in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

INFO: [SIM-utils-51] Simulation object is 'sim\_1'

INFO: [SIM-utils-54] Inspecting design source files for 'decode\_tb' in fileset 'sim\_1'...

INFO: [USF-XSim-97] Finding global include files...

INFO: [USF-XSim-98] Fetching design files from 'sim\_1'...

INFO: [USF-XSim-2] XSim::Compile design

INFO: [USF-XSim-61] Executing 'COMPILE and ANALYZE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xvlog --incr --relax -prj decode\_tb\_vlog.prj"

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module decode

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode\_tb.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module decode\_tb

INFO: [USF-XSim-69] 'compile' step finished in '3' seconds

INFO: [USF-XSim-3] XSim::Elaborate design

INFO: [USF-XSim-61] Executing 'ELABORATE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xelab -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot decode\_tb\_behav xil\_defaultlib.decode\_tb xil\_defaultlib.glbl -log elaborate.log"

Vivado Simulator 2019.2

Copyright 1986-1999, 2001-2019 Xilinx, Inc. All Rights Reserved.

Running: F:/Xilinx/Vivado/2019.2/bin/unwrapped/win64.o/xelab.exe -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot decode\_tb\_behav xil\_defaultlib.decode\_tb xil\_defaultlib.glbl -log elaborate.log

Using 2 slave threads.

Starting static elaboration

Pass Through NonSizing Optimizer

Completed static elaboration

Starting simulation data flow analysis

WARNING: [XSIM 43-4100] "F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/glbl.v" Line 6. Module glbl has a timescale but at least one module in design doesn't have timescale.

Completed simulation data flow analysis

Time Resolution for simulation is 1ps

Compiling module xil\_defaultlib.decode

Compiling module xil\_defaultlib.decode\_tb

Compiling module xil\_defaultlib.glbl

Built simulation snapshot decode\_tb\_behav

run\_program: Time (s): cpu = 00:00:00 ; elapsed = 00:00:08 . Memory (MB): peak = 865.594 ; gain = 0.000

INFO: [USF-XSim-69] 'elaborate' step finished in '7' seconds

INFO: [USF-XSim-4] XSim::Simulate design

INFO: [USF-XSim-61] Executing 'SIMULATE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

INFO: [USF-XSim-98] \*\*\* Running xsim

with args "decode\_tb\_behav -key {Behavioral:sim\_1:Functional:decode\_tb} -tclbatch {decode\_tb.tcl} -view {F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/top\_tb\_behav.wcfg} -log {simulate.log}"

INFO: [USF-XSim-8] Loading simulator feature

Vivado Simulator 2019.2

Time resolution is 1 ps

open\_wave\_config F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/top\_tb\_behav.wcfg

WARNING: Simulation object /top\_tb/clock was not found in the design.

WARNING: Simulation object /top\_tb/reset was not found in the design.

WARNING: Simulation object /top\_tb/result was not found in the design.

WARNING: Simulation object /top\_tb/x was not found in the design.

source decode\_tb.tcl

# set curr\_wave [current\_wave\_config]

# if { [string length $curr\_wave] == 0 } {

# if { [llength [get\_objects]] > 0} {

# add\_wave /

# set\_property needs\_save false [current\_wave\_config]

# } else {

# send\_msg\_id Add\_Wave-1 WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window go to 'File->New Waveform Configuration' or type 'create\_wave\_config' in the TCL console."

# }

# }

# run 1000ns

Starting Decode Test

--------------------------------------------------------------------------------

addi zero, zero, 0

Time: 10

instruction: 00000000000000000000000000010011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 0

read\_sel2: 0

write\_sel: 0

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

addi a1, zero, -1

Time: 20

instruction: 11111111111100000000010110010011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0003

read\_sel1: 0

read\_sel2: 31

write\_sel: 11

wEn: 1

branch\_op: 0

imm32: 11111111111111111111111111111111

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

add a6, a1, a2

Time: 30

instruction: 00000000110001011000100000110011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 11

read\_sel2: 12

write\_sel: 16

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

sub a7, a2, a4

Time: 40

instruction: 01000000111001100000100010110011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 12

read\_sel2: 14

write\_sel: 17

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 001000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

slt a0, a1, a5

Time: 50

instruction: 00000000111101011010010100110011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 11

read\_sel2: 15

write\_sel: 10

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 000010

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

xor a4, a1, a5

Time: 60

instruction: 00000000111101011100011100110011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 11

read\_sel2: 15

write\_sel: 14

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 000100

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

and a3, a3, a1

Time: 70

instruction: 00000000101101101111011010110011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 13

read\_sel2: 11

write\_sel: 13

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 000111

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

addi a1, zero, 1536

Time: 80

instruction: 01100000000000000000010110010011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0604

read\_sel1: 0

read\_sel2: 0

write\_sel: 11

wEn: 1

branch\_op: 0

imm32: 00000000000000000000011000000000

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

sw a2, 0(a1)

Time: 90

instruction: 00000000110001011010000000100011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 11

read\_sel2: 12

write\_sel: 0

wEn: 0

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 1

wb\_sel: 0

--------------------------------------------------------------------------------

lw s2, 0(a1)

Time: 100

instruction: 00000000000001011010100100000011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 11

read\_sel2: 0

write\_sel: 18

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 1

--------------------------------------------------------------------------------

jal zero,128

Time: 110

instruction: 00000001010000000000000001101111

PC: 0114

JALR\_target: 0000

branch 0

next\_PC\_sel 1

target\_PC 012c

read\_sel1: 0

read\_sel2: 20

write\_sel: 0

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000000010100

op\_A\_sel: 10

op\_B\_sel: 1

ALU\_Control: 011111

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

jalr ra,196(ra)

Time: 120

instruction: 00001100010000001000000011100111

PC: 0094

JALR\_target: 0154

branch 0

next\_PC\_sel 1

target\_PC 0154

read\_sel1: 1

read\_sel2: 4

write\_sel: 1

wEn: 1

branch\_op: 0

imm32: 00000000000000000000000011000100

op\_A\_sel: 10

op\_B\_sel: 1

ALU\_Control: 111111

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

BEQ x1, x2

Time: 130

instruction: 00000000001000001000100001100011

PC: 0004

JALR\_target: 0154

branch 0

next\_PC\_sel 0

target\_PC 0014

read\_sel1: 1

read\_sel2: 2

write\_sel: 16

wEn: 0

branch\_op: 1

imm32: 00000000000000000000000000010000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 010000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

BEQ x1, x2 - taken

Time: 140

instruction: 00000000001000001000100001100011

PC: 0008

JALR\_target: 0154

branch 1

next\_PC\_sel 1

target\_PC 0018

read\_sel1: 1

read\_sel2: 2

write\_sel: 16

wEn: 0

branch\_op: 1

imm32: 00000000000000000000000000010000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 010000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

LUI rd, DEADB

Time: 150

instruction: 11011110101011011011000110110111

PC: 0000

JALR\_target: 0154

branch 0

next\_PC\_sel 0

target\_PC b004

read\_sel1: 0

read\_sel2: 10

write\_sel: 3

wEn: 1

branch\_op: 0

imm32: 11011110101011011011000000000000

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

AUIPC rd, DEADB (Note PC = 0004 to begin

Time: 160

instruction: 11011110101011011011000110010111

PC: 0004

JALR\_target: 0154

branch 0

next\_PC\_sel 0

target\_PC b008

read\_sel1: 27

read\_sel2: 10

write\_sel: 3

wEn: 1

branch\_op: 0

imm32: 11011110101011011011000000000000

op\_A\_sel: 01

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

$stop called at time : 170 ns : File "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode\_tb.v" Line 227

INFO: [USF-XSim-96] XSim completed. Design snapshot 'decode\_tb\_behav' loaded.

INFO: [USF-XSim-97] XSim simulation ran for 1000ns

launch\_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:16 . Memory (MB): peak = 865.594 ; gain = 0.000

close\_sim

INFO: [Simtcl 6-16] Simulation closed

launch\_simulation

Command: launch\_simulation

INFO: [Vivado 12-5682] Launching behavioral simulation in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

INFO: [SIM-utils-51] Simulation object is 'sim\_1'

INFO: [SIM-utils-54] Inspecting design source files for 'decode\_tb' in fileset 'sim\_1'...

INFO: [USF-XSim-97] Finding global include files...

INFO: [USF-XSim-98] Fetching design files from 'sim\_1'...

INFO: [USF-XSim-2] XSim::Compile design

INFO: [USF-XSim-61] Executing 'COMPILE and ANALYZE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xvlog --incr --relax -prj decode\_tb\_vlog.prj"

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module decode

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode\_tb.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module decode\_tb

INFO: [USF-XSim-69] 'compile' step finished in '3' seconds

INFO: [USF-XSim-3] XSim::Elaborate design

INFO: [USF-XSim-61] Executing 'ELABORATE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xelab -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot decode\_tb\_behav xil\_defaultlib.decode\_tb xil\_defaultlib.glbl -log elaborate.log"

Vivado Simulator 2019.2

Copyright 1986-1999, 2001-2019 Xilinx, Inc. All Rights Reserved.

Running: F:/Xilinx/Vivado/2019.2/bin/unwrapped/win64.o/xelab.exe -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot decode\_tb\_behav xil\_defaultlib.decode\_tb xil\_defaultlib.glbl -log elaborate.log

Using 2 slave threads.

Starting static elaboration

Pass Through NonSizing Optimizer

ERROR: [VRFC 10-3180] cannot find port 'imm32' on this module [F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode\_tb.v:63]

ERROR: [XSIM 43-3322] Static elaboration of top level Verilog design unit(s) in library work failed.

INFO: [USF-XSim-69] 'elaborate' step finished in '3' seconds

INFO: [USF-XSim-99] Step results log file:'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/elaborate.log'

ERROR: [USF-XSim-62] 'elaborate' step failed with error(s). Please check the Tcl console output or 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/elaborate.log' file for more information.

ERROR: [Vivado 12-4473] Detected error while running simulation. Please correct the issue and retry this operation.

launch\_simulation: Time (s): cpu = 00:00:00 ; elapsed = 00:00:06 . Memory (MB): peak = 865.594 ; gain = 0.000

ERROR: [Common 17-39] 'launch\_simulation' failed due to earlier errors.

reset\_simulation -simset sim\_1 -mode behavioral

INFO: [Vivado 12-2266] Removing simulation data...

INFO: [Vivado 12-2267] Reset complete

launch\_simulation

Command: launch\_simulation

INFO: [Vivado 12-5682] Launching behavioral simulation in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

INFO: [SIM-utils-51] Simulation object is 'sim\_1'

INFO: [SIM-utils-54] Inspecting design source files for 'decode\_tb' in fileset 'sim\_1'...

INFO: [USF-XSim-97] Finding global include files...

INFO: [USF-XSim-98] Fetching design files from 'sim\_1'...

INFO: [USF-XSim-2] XSim::Compile design

INFO: [USF-XSim-61] Executing 'COMPILE and ANALYZE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xvlog --incr --relax -prj decode\_tb\_vlog.prj"

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module decode

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode\_tb.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module decode\_tb

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/glbl.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module glbl

INFO: [USF-XSim-69] 'compile' step finished in '3' seconds

INFO: [USF-XSim-3] XSim::Elaborate design

INFO: [USF-XSim-61] Executing 'ELABORATE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xelab -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot decode\_tb\_behav xil\_defaultlib.decode\_tb xil\_defaultlib.glbl -log elaborate.log"

Vivado Simulator 2019.2

Copyright 1986-1999, 2001-2019 Xilinx, Inc. All Rights Reserved.

Running: F:/Xilinx/Vivado/2019.2/bin/unwrapped/win64.o/xelab.exe -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot decode\_tb\_behav xil\_defaultlib.decode\_tb xil\_defaultlib.glbl -log elaborate.log

Using 2 slave threads.

Starting static elaboration

Pass Through NonSizing Optimizer

ERROR: [VRFC 10-3180] cannot find port 'imm32' on this module [F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode\_tb.v:63]

ERROR: [XSIM 43-3322] Static elaboration of top level Verilog design unit(s) in library work failed.

INFO: [USF-XSim-69] 'elaborate' step finished in '3' seconds

INFO: [USF-XSim-99] Step results log file:'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/elaborate.log'

ERROR: [USF-XSim-62] 'elaborate' step failed with error(s). Please check the Tcl console output or 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/elaborate.log' file for more information.

ERROR: [Vivado 12-4473] Detected error while running simulation. Please correct the issue and retry this operation.

launch\_simulation: Time (s): cpu = 00:00:00 ; elapsed = 00:00:06 . Memory (MB): peak = 865.594 ; gain = 0.000

ERROR: [Common 17-39] 'launch\_simulation' failed due to earlier errors.

launch\_simulation

Command: launch\_simulation

INFO: [Vivado 12-5682] Launching behavioral simulation in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

INFO: [SIM-utils-51] Simulation object is 'sim\_1'

INFO: [SIM-utils-54] Inspecting design source files for 'decode\_tb' in fileset 'sim\_1'...

INFO: [USF-XSim-97] Finding global include files...

INFO: [USF-XSim-98] Fetching design files from 'sim\_1'...

INFO: [USF-XSim-2] XSim::Compile design

INFO: [USF-XSim-61] Executing 'COMPILE and ANALYZE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xvlog --incr --relax -prj decode\_tb\_vlog.prj"

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module decode

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode\_tb.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module decode\_tb

INFO: [USF-XSim-69] 'compile' step finished in '3' seconds

INFO: [USF-XSim-3] XSim::Elaborate design

INFO: [USF-XSim-61] Executing 'ELABORATE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xelab -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot decode\_tb\_behav xil\_defaultlib.decode\_tb xil\_defaultlib.glbl -log elaborate.log"

Vivado Simulator 2019.2

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Running: F:/Xilinx/Vivado/2019.2/bin/unwrapped/win64.o/xelab.exe -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot decode\_tb\_behav xil\_defaultlib.decode\_tb xil\_defaultlib.glbl -log elaborate.log

Using 2 slave threads.

Starting static elaboration

Pass Through NonSizing Optimizer

ERROR: [VRFC 10-2989] 'imm32' is not declared [F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode\_tb.v:93]

ERROR: [XSIM 43-3322] Static elaboration of top level Verilog design unit(s) in library work failed.

INFO: [USF-XSim-69] 'elaborate' step finished in '3' seconds

INFO: [USF-XSim-99] Step results log file:'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/elaborate.log'

ERROR: [USF-XSim-62] 'elaborate' step failed with error(s). Please check the Tcl console output or 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/elaborate.log' file for more information.

ERROR: [Vivado 12-4473] Detected error while running simulation. Please correct the issue and retry this operation.

launch\_simulation: Time (s): cpu = 00:00:01 ; elapsed = 00:00:06 . Memory (MB): peak = 865.594 ; gain = 0.000

ERROR: [Common 17-39] 'launch\_simulation' failed due to earlier errors.

reset\_simulation -simset sim\_1 -mode behavioral

INFO: [Vivado 12-2266] Removing simulation data...

INFO: [Vivado 12-2267] Reset complete

launch\_simulation

Command: launch\_simulation

INFO: [Vivado 12-5682] Launching behavioral simulation in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

INFO: [SIM-utils-51] Simulation object is 'sim\_1'

INFO: [SIM-utils-54] Inspecting design source files for 'decode\_tb' in fileset 'sim\_1'...

INFO: [USF-XSim-97] Finding global include files...

INFO: [USF-XSim-98] Fetching design files from 'sim\_1'...

INFO: [USF-XSim-2] XSim::Compile design

INFO: [USF-XSim-61] Executing 'COMPILE and ANALYZE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xvlog --incr --relax -prj decode\_tb\_vlog.prj"

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module decode

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode\_tb.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module decode\_tb

INFO: [VRFC 10-2263] Analyzing Verilog file "F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/glbl.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module glbl

INFO: [USF-XSim-69] 'compile' step finished in '3' seconds

INFO: [USF-XSim-3] XSim::Elaborate design

INFO: [USF-XSim-61] Executing 'ELABORATE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

"xelab -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot decode\_tb\_behav xil\_defaultlib.decode\_tb xil\_defaultlib.glbl -log elaborate.log"

Vivado Simulator 2019.2

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Running: F:/Xilinx/Vivado/2019.2/bin/unwrapped/win64.o/xelab.exe -wto c4c0617f01aa4542bd003cc14ce0977e --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot decode\_tb\_behav xil\_defaultlib.decode\_tb xil\_defaultlib.glbl -log elaborate.log

Using 2 slave threads.

Starting static elaboration

Pass Through NonSizing Optimizer

Completed static elaboration

Starting simulation data flow analysis

WARNING: [XSIM 43-4100] "F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/glbl.v" Line 6. Module glbl has a timescale but at least one module in design doesn't have timescale.

Completed simulation data flow analysis

Time Resolution for simulation is 1ps

Compiling module xil\_defaultlib.decode

Compiling module xil\_defaultlib.decode\_tb

Compiling module xil\_defaultlib.glbl

Built simulation snapshot decode\_tb\_behav

\*\*\*\*\*\* Webtalk v2019.2 (64-bit)

\*\*\*\* SW Build 2708876 on Wed Nov 6 21:40:23 MST 2019

\*\*\*\* IP Build 2700528 on Thu Nov 7 00:09:20 MST 2019

\*\* Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.

source F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/xsim.dir/decode\_tb\_behav/webtalk/xsim\_webtalk.tcl -notrace

INFO: [Common 17-186] 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim/xsim.dir/decode\_tb\_behav/webtalk/usage\_statistics\_ext\_xsim.xml' has been successfully sent to Xilinx on Sun Jul 4 21:28:06 2021. For additional details about this file, please refer to the WebTalk help file at F:/Xilinx/Vivado/2019.2/doc/webtalk\_introduction.html.

INFO: [Common 17-206] Exiting Webtalk at Sun Jul 4 21:28:06 2021...

run\_program: Time (s): cpu = 00:00:00 ; elapsed = 00:00:13 . Memory (MB): peak = 865.594 ; gain = 0.000

INFO: [USF-XSim-69] 'elaborate' step finished in '14' seconds

INFO: [USF-XSim-4] XSim::Simulate design

INFO: [USF-XSim-61] Executing 'SIMULATE' step in 'F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR.sim/sim\_1/behav/xsim'

INFO: [USF-XSim-98] \*\*\* Running xsim

with args "decode\_tb\_behav -key {Behavioral:sim\_1:Functional:decode\_tb} -tclbatch {decode\_tb.tcl} -view {F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/top\_tb\_behav.wcfg} -log {simulate.log}"

INFO: [USF-XSim-8] Loading simulator feature

Vivado Simulator 2019.2

Time resolution is 1 ps

open\_wave\_config F:/Users/ASUS/VE370\_P2\_RISC-V\_SINGLE\_PROCESSOR/top\_tb\_behav.wcfg

WARNING: Simulation object /top\_tb/clock was not found in the design.

WARNING: Simulation object /top\_tb/reset was not found in the design.

WARNING: Simulation object /top\_tb/result was not found in the design.

WARNING: Simulation object /top\_tb/x was not found in the design.

source decode\_tb.tcl

# set curr\_wave [current\_wave\_config]

# if { [string length $curr\_wave] == 0 } {

# if { [llength [get\_objects]] > 0} {

# add\_wave /

# set\_property needs\_save false [current\_wave\_config]

# } else {

# send\_msg\_id Add\_Wave-1 WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window go to 'File->New Waveform Configuration' or type 'create\_wave\_config' in the TCL console."

# }

# }

# run 1000ns

Starting Decode Test

--------------------------------------------------------------------------------

addi zero, zero, 0

Time: 10

instruction: 00000000000000000000000000010011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 0

read\_sel2: 0

write\_sel: 0

wEn: 1

branch\_op: 0

imm64: 0000000000000000000000000000000000000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

addi a1, zero, -1

Time: 20

instruction: 11111111111100000000010110010011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0003

read\_sel1: 0

read\_sel2: 31

write\_sel: 11

wEn: 1

branch\_op: 0

imm64: 1111111111111111111111111111111111111111111111111111111111111111

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

add a6, a1, a2

Time: 30

instruction: 00000000110001011000100000110011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 11

read\_sel2: 12

write\_sel: 16

wEn: 1

branch\_op: 0

imm64: 0000000000000000000000000000000000000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

sub a7, a2, a4

Time: 40

instruction: 01000000111001100000100010110011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 12

read\_sel2: 14

write\_sel: 17

wEn: 1

branch\_op: 0

imm64: 0000000000000000000000000000000000000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 001000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

slt a0, a1, a5

Time: 50

instruction: 00000000111101011010010100110011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 11

read\_sel2: 15

write\_sel: 10

wEn: 1

branch\_op: 0

imm64: 0000000000000000000000000000000000000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 000010

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

xor a4, a1, a5

Time: 60

instruction: 00000000111101011100011100110011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 11

read\_sel2: 15

write\_sel: 14

wEn: 1

branch\_op: 0

imm64: 0000000000000000000000000000000000000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 000100

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

and a3, a3, a1

Time: 70

instruction: 00000000101101101111011010110011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 13

read\_sel2: 11

write\_sel: 13

wEn: 1

branch\_op: 0

imm64: 0000000000000000000000000000000000000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 000111

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

addi a1, zero, 1536

Time: 80

instruction: 01100000000000000000010110010011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0604

read\_sel1: 0

read\_sel2: 0

write\_sel: 11

wEn: 1

branch\_op: 0

imm64: 0000000000000000000000000000000000000000000000000000011000000000

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

sw a2, 0(a1)

Time: 90

instruction: 00000000110001011010000000100011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 11

read\_sel2: 12

write\_sel: 0

wEn: 0

branch\_op: 0

imm64: 0000000000000000000000000000000000000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 1

wb\_sel: 0

--------------------------------------------------------------------------------

lw s2, 0(a1)

Time: 100

instruction: 00000000000001011010100100000011

PC: 0000

JALR\_target: 0000

branch 0

next\_PC\_sel 0

target\_PC 0004

read\_sel1: 11

read\_sel2: 0

write\_sel: 18

wEn: 1

branch\_op: 0

imm64: 0000000000000000000000000000000000000000000000000000000000000000

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 1

--------------------------------------------------------------------------------

jal zero,128

Time: 110

instruction: 00000001010000000000000001101111

PC: 0114

JALR\_target: 0000

branch 0

next\_PC\_sel 1

target\_PC 012c

read\_sel1: 0

read\_sel2: 20

write\_sel: 0

wEn: 1

branch\_op: 0

imm64: 0000000000000000000000000000000000000000000000000000000000010100

op\_A\_sel: 10

op\_B\_sel: 1

ALU\_Control: 011111

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

jalr ra,196(ra)

Time: 120

instruction: 00001100010000001000000011100111

PC: 0094

JALR\_target: 0154

branch 0

next\_PC\_sel 1

target\_PC 0154

read\_sel1: 1

read\_sel2: 4

write\_sel: 1

wEn: 1

branch\_op: 0

imm64: 0000000000000000000000000000000000000000000000000000000011000100

op\_A\_sel: 10

op\_B\_sel: 1

ALU\_Control: 111111

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

BEQ x1, x2

Time: 130

instruction: 00000000001000001000100001100011

PC: 0004

JALR\_target: 0154

branch 0

next\_PC\_sel 0

target\_PC 0014

read\_sel1: 1

read\_sel2: 2

write\_sel: 16

wEn: 0

branch\_op: 1

imm64: 0000000000000000000000000000000000000000000000000000000000010000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 010000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

BEQ x1, x2 - taken

Time: 140

instruction: 00000000001000001000100001100011

PC: 0008

JALR\_target: 0154

branch 1

next\_PC\_sel 1

target\_PC 0018

read\_sel1: 1

read\_sel2: 2

write\_sel: 16

wEn: 0

branch\_op: 1

imm64: 0000000000000000000000000000000000000000000000000000000000010000

op\_A\_sel: 00

op\_B\_sel: 0

ALU\_Control: 010000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

LUI rd, DEADB

Time: 150

instruction: 11011110101011011011000110110111

PC: 0000

JALR\_target: 0154

branch 0

next\_PC\_sel 0

target\_PC b004

read\_sel1: 0

read\_sel2: 10

write\_sel: 3

wEn: 1

branch\_op: 0

imm64: 0000000000000000000000000000000011011110101011011011000000000000

op\_A\_sel: 00

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

AUIPC rd, DEADB (Note PC = 0004 to begin

Time: 160

instruction: 11011110101011011011000110010111

PC: 0004

JALR\_target: 0154

branch 0

next\_PC\_sel 0

target\_PC b008

read\_sel1: 27

read\_sel2: 10

write\_sel: 3

wEn: 1

branch\_op: 0

imm64: 0000000000000000000000000000000011011110101011011011000000000000

op\_A\_sel: 01

op\_B\_sel: 1

ALU\_Control: 000000

mem\_wEn: 0

wb\_sel: 0

--------------------------------------------------------------------------------

$stop called at time : 170 ns : File "F:/Users/ASUS/RISC-V-Processor-master/RISC-V-Processor-master/RISCV\_Single\_Cycle\_Processor/RISCV\_Single\_Cycle\_Processor.srcs/sources\_1/RISC-V-Processor-master/decode\_tb.v" Line 230

INFO: [USF-XSim-96] XSim completed. Design snapshot 'decode\_tb\_behav' loaded.

INFO: [USF-XSim-97] XSim simulation ran for 1000ns

launch\_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:21 . Memory (MB): peak = 874.422 ; gain = 8.828